LM13700 Dual Operational Transconductance Amplifiers with Linearizing Diodes and Buffers

Check for Samples: LM13700

FEATURES

- **g_m Adjustable over 6 Decades**
- **Excellent g_m Linearity**
- **Excellent Matching between Amplifiers**
- **Linearizing Diodes**
- **High Impedance Buffers**
- **High Output Signal-to-Noise Ratio**

APPLICATIONS

- **Current-Controlled Amplifiers**
- **Current-Controlled Impedances**
- **Current-Controlled Filters**
- **Current-Controlled Oscillators**
- **Multiplexers**
- **Timers**
- **Sample-and-Hold circuits**

DESCRIPTION

The LM13700 series consists of two current controlled transconductance amplifiers, each with differential inputs and a push-pull output. The two amplifiers share common supplies but otherwise operate independently. Linearizing diodes are provided at the inputs to reduce distortion and allow higher input levels. The result is a 10 dB signal-to-noise improvement referenced to 0.5 percent THD. High impedance buffers are provided which are especially designed to complement the dynamic range of the amplifiers. The output buffers of the LM13700 differ from those of the LM13600 in that their input bias currents (and hence their output DC levels) are independent of I_{ABC}. This may result in performance superior to that of the LM13600 in audio applications.

Connection Diagram

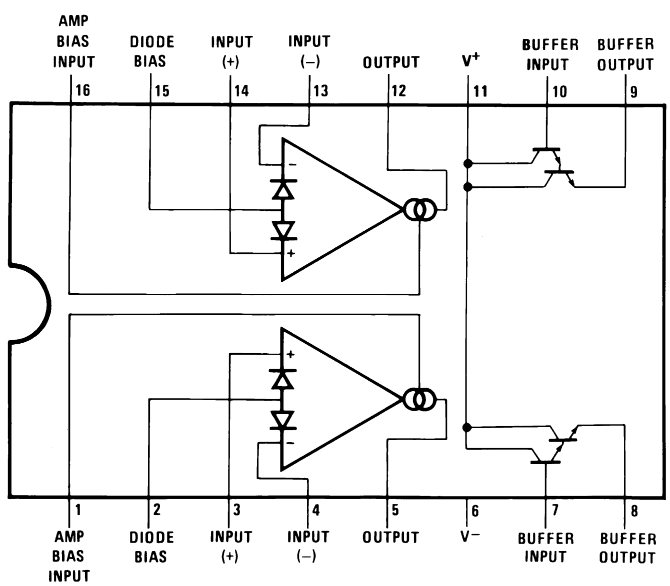


Figure 1. PDIP and SOIC Packages-Top View
See Package Number D0016A or NFG0016E

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [1]

Supply Voltage	
LM13700	36 V_{DC} or ±18V
Power Dissipation [2] T_A = 25°C	
LM13700N	570 mW
Differential Input Voltage	±5V
Diode Bias Current (I_D)	2 mA
Amplifier Bias Current (I_{ABC})	2 mA
Output Short Circuit Duration	Continuous
Buffer Output Current [3]	20 mA
Operating Temperature Range	
LM13700N	0°C to +70°C
DC Input Voltage	$+V_S$ to $-V_S$
Storage Temperature Range	−65°C to +150°C
Soldering Information	
PDIP Package	
Soldering (10 sec.)	260°C
SOIC Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

(1) “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits.
(2) For operation at ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance, junction to ambient, as follows: LM13700N, 90°C/W; LM13700M, 110°C/W.
(3) Buffer output current should be limited so as to not exceed package dissipation.

Electrical Characteristics (1)

Parameter	Test Conditions	LM13700			Units
		Min	Typ	Max	
Input Offset Voltage (V_{OS})	Over Specified Temperature Range		0.4	4	mV
	I_{ABC} = 5 µA		0.3	4	
V_{OS} Including Diodes	Diode Bias Current (I_D) = 500 µA		0.5	5	mV
Input Offset Change	5 µA ≤ I_{ABC} ≤ 500 µA		0.1	3	mV
Input Offset Current			0.1	0.6	µA
Input Bias Current	Over Specified Temperature Range		0.4	5	µA
			1	8	
Forward Transconductance (g_m)		6700	9600	13000	µmho
	Over Specified Temperature Range	5400			
g_m Tracking			0.3		dB
Peak Output Current	R_L = 0, I_{ABC} = 5 µA		5		µA
	R_L = 0, I_{ABC} = 500 µA	350	500	650	
	R_L = 0, Over Specified Temp Range	300			
Peak Output Voltage					
Positive	R_L = ∞, 5 µA ≤ I_{ABC} ≤ 500 µA	+12	+14.2		V
Negative	R_L = ∞, 5 µA ≤ I_{ABC} ≤ 500 µA	−12	−14.4		V
Supply Current	I_{ABC} = 500 µA, Both Channels		2.6		mA
V_{OS} Sensitivity					
Positive	**$\Delta V_{OS}/\Delta V^+$**		20	150	µV/V
Negative	**$\Delta V_{OS}/\Delta V^-$**		20	150	µV/V
CMRR		80	110		dB
Common Mode Range		±12	±13.5		V
Crosstalk	Referred to Input (2) 20 Hz < f < 20 kHz		100		dB
Differential Input Current	I_{ABC} = 0, Input = ±4V		0.02	100	nA
Leakage Current	I_{ABC} = 0 (Refer to Test Circuit)		0.2	100	nA
Input Resistance		10	26		kΩ
Open Loop Bandwidth			2		MHz
Slew Rate	Unity Gain Compensated		50		V/µs
Buffer Input Current	(2)		0.5	2	µA
Peak Buffer Output Voltage	(2)	10			V

(1) These specifications apply for V_S = ±15V, T_A = 25°C, amplifier bias current (I_{ABC}) = 500 µA, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.
(2) These specifications apply for V_S = ±15V, I_{ABC} = 500 µA, R_{OUT} = 5 kΩ connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.

Schematic Diagram

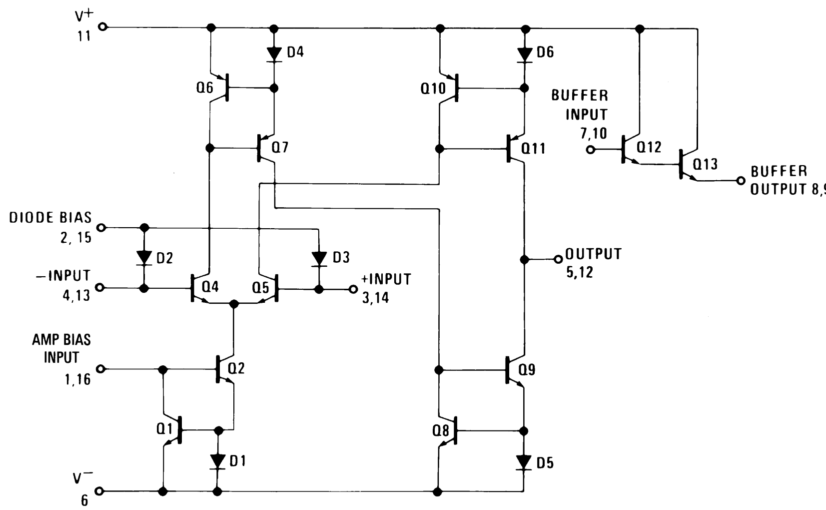


Figure 2. One Operational Transconductance Amplifier

Typical Application

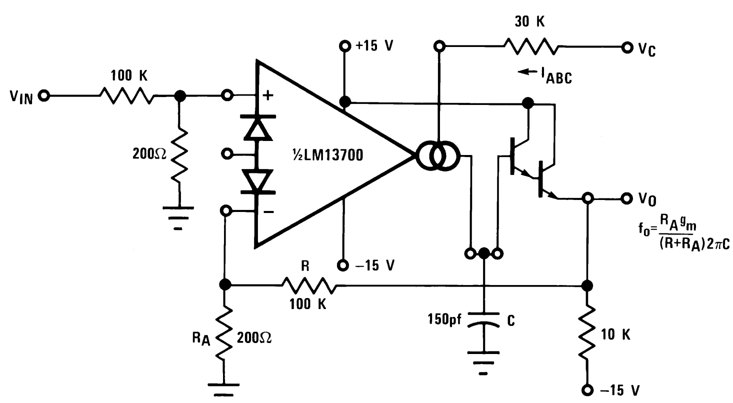


Figure 3. Voltage Controlled Low-Pass Filter

Typical Performance Characteristics

Input Offset Voltage

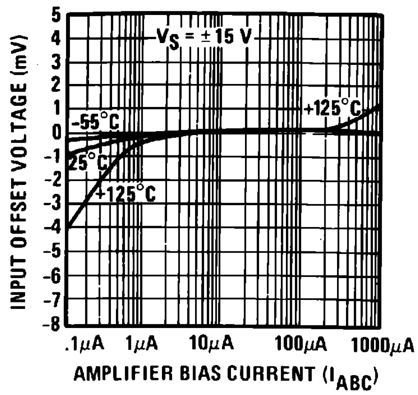


Figure 4.

Input Offset Current

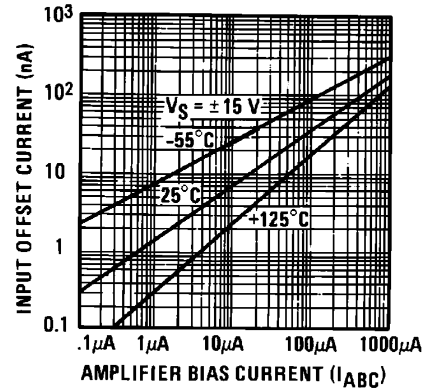


Figure 5.

Input Bias Current

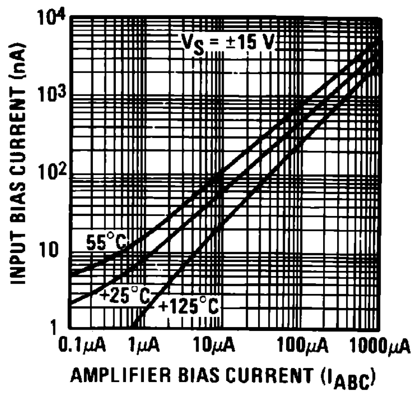


Figure 6.

Peak Output Current

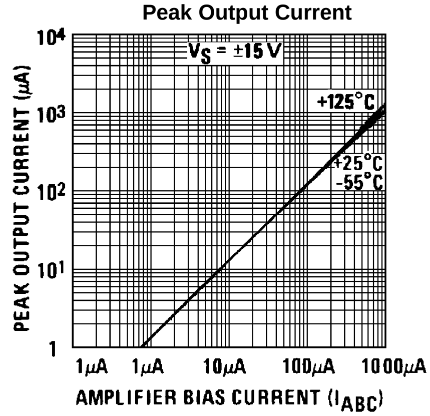


Figure 7.

Peak Output Voltage and Common Mode Range

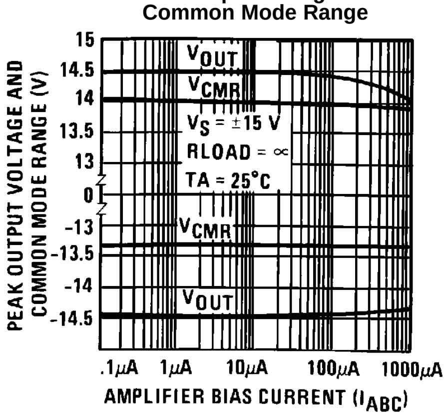


Figure 8.

Leakage Current

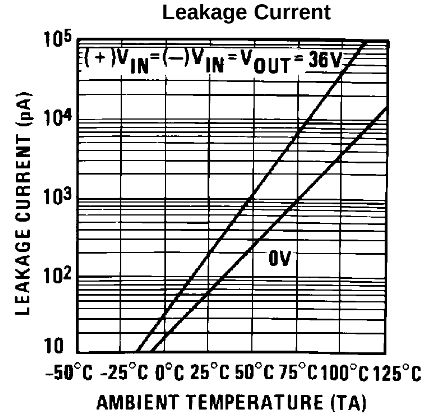


Figure 9.

Typical Performance Characteristics (continued)

Input Leakage

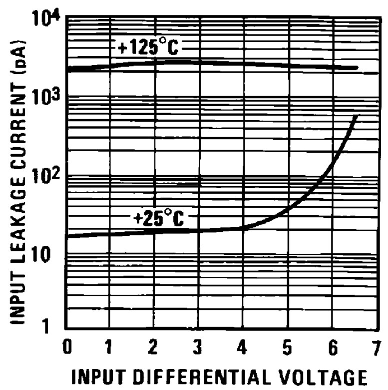


Figure 10.

Transconductance

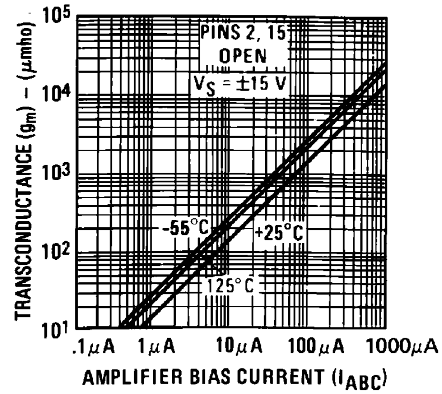


Figure 11.

Input Resistance

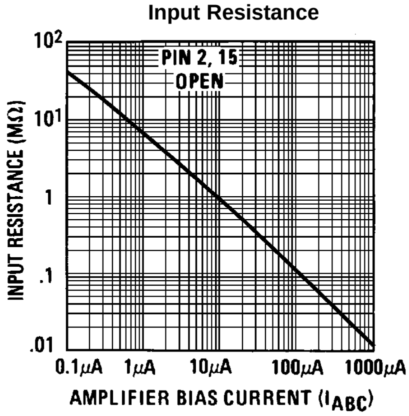


Figure 12.

Amplifier Bias Voltage vs. Amplifier Bias Current

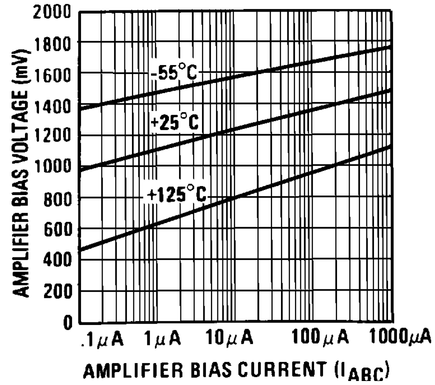


Figure 13.

Input and Output Capacitance

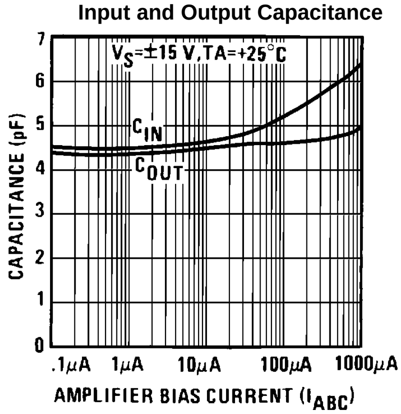


Figure 14.

Output Resistance

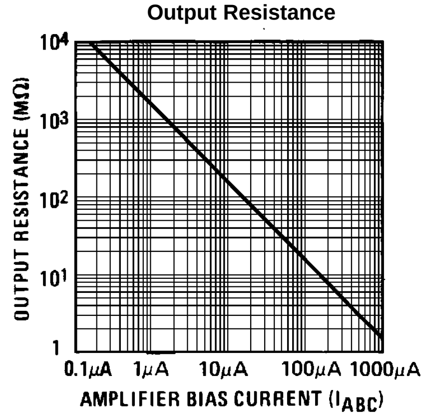


Figure 15.

Typical Performance Characteristics (continued)

Distortion vs. Differential Input Voltage

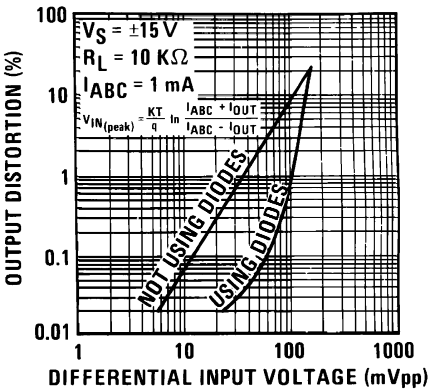


Figure 16.

Voltage vs. Amplifier Bias Current

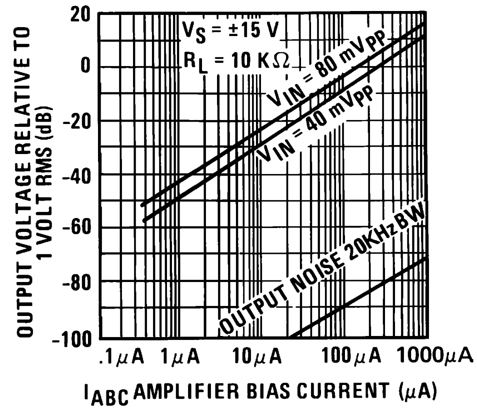


Figure 17.

Output Noise vs. Frequency

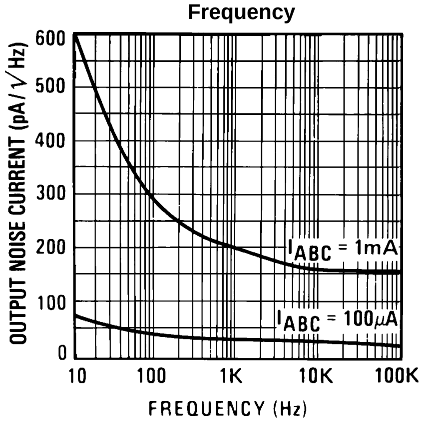


Figure 18.

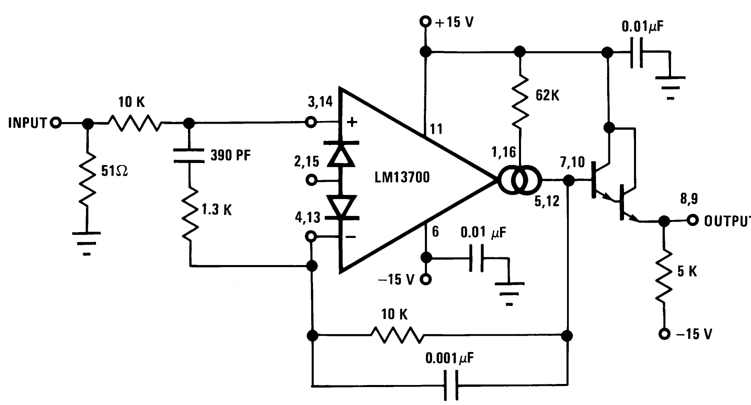


Figure 19. Unity Gain Follower

Typical Performance Characteristics (continued)

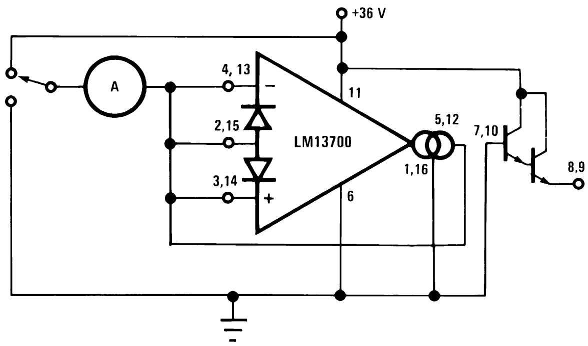


Figure 20. Leakage Current Test Circuit

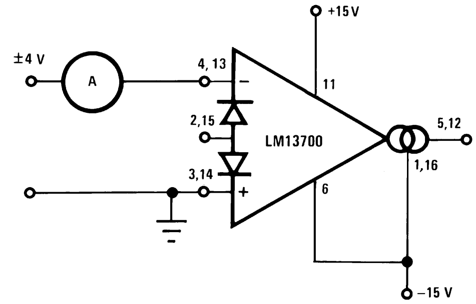


Figure 21. Differential Input Current Test Circuit

Circuit Description

The differential transistor pair Q_4 and Q_5 form a transconductance stage in that the ratio of their collector currents is defined by the differential input voltage according to the transfer function:

$$V_{IN} = \frac{kT}{q} \ln \frac{I_5}{I_4} \tag{1}$$

where V_{IN} is the differential input voltage, kT/q is approximately 26 mV at 25°C and I_5 and I_4 are the collector currents of transistors Q_5 and Q_4 respectively. With the exception of Q_{12} and Q_{13}, all transistors and diodes are identical in size. Transistors Q_1 and Q_2 with Diode D_1 form a current mirror which forces the sum of currents I_4 and I_5 to equal I_{ABC}:

$$I_4 + I_5 = I_{ABC} \tag{2}$$

where I_{ABC} is the amplifier bias current applied to the gain pin.

For small differential input voltages the ratio of I_4 and I_5 approaches unity and the Taylor series of the In function can be approximated as:

$$\frac{kT}{q} \ln \frac{I_5}{I_4} \approx \frac{kT}{q} \frac{I_5 - I_4}{I_4}$$

$$I_4 \approx I_5 \approx \frac{I_{ABC}}{2} \tag{3}$$

$$V_{IN}\left[\frac{I_{ABC}q}{2kT}\right] = I_5 - I_4 \tag{4}$$

Collector currents I_4 and I_5 are not very useful by themselves and it is necessary to subtract one current from the other. The remaining transistors and diodes form three current mirrors that produce an output current equal to I_5 minus I_4 thus:

$$V_{IN}\left[\frac{I_{ABC}q}{2kT}\right] = I_{OUT} \tag{5}$$

The term in brackets is then the transconductance of the amplifier and is proportional to I_{ABC}.

Linearizing Diodes

For differential voltages greater than a few millivolts, Equation 3 becomes less valid and the transconductance becomes increasingly nonlinear. Figure 22 demonstrates how the internal diodes can linearize the transfer function of the amplifier. For convenience assume the diodes are biased with current sources and the input signal is in the form of current I_S. Since the sum of I_4 and I_5 is I_{ABC} and the difference is I_{OUT}, currents I_4 and I_5 can be written as follows:

$$I_4 = \frac{I_{ABC}}{2} - \frac{I_{OUT}}{2},\ I_5 = \frac{I_{ABC}}{2} + \frac{I_{OUT}}{2} \tag{6}$$

Since the diodes and the input transistors have identical geometries and are subject to similar voltages and temperatures, the following is true:

$$\frac{kT}{q}\ln\frac{\frac{I_D}{2}+I_S}{\frac{I_D}{2}-I_S}=\frac{kT}{q}\ln\frac{\frac{I_{ABC}}{2}+\frac{I_{OUT}}{2}}{\frac{I_{ABC}}{2}-\frac{I_{OUT}}{2}}$$

$$\therefore I_{OUT}=I_S\left(\frac{2I_{ABC}}{I_D}\right)\text{ for }|I_S|<\frac{I_D}{2} \tag{7}$$

Notice that in deriving Equation 7 no approximations have been made and there are no temperature-dependent terms. The limitations are that the signal current not exceed $I_D/2$ and that the diodes be biased with currents. In practice, replacing the current sources with resistors will generate insignificant errors.

APPLICATIONS

Voltage Controlled Amplifiers

Figure 23 shows how the linearizing diodes can be used in a voltage-controlled amplifier. To understand the input biasing, it is best to consider the 13 kΩ resistor as a current source and use a Thevenin equivalent circuit as shown in Figure 24. This circuit is similar to Figure 22 and operates the same. The potentiometer in Figure 23 is adjusted to minimize the effects of the control signal at the output.

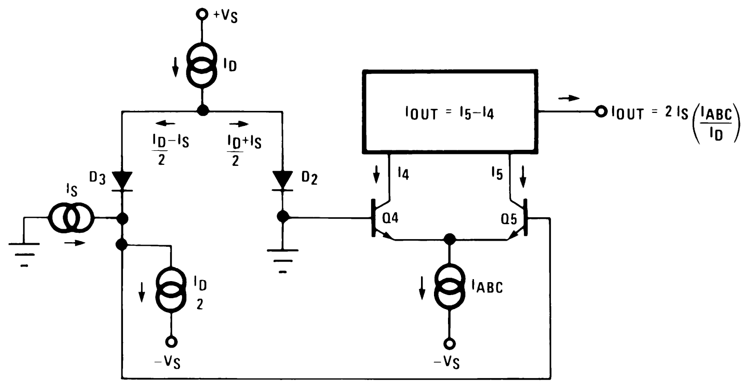


Figure 22. Linearizing Diodes

For optimum signal-to-noise performance, I_{ABC} should be as large as possible as shown by the Output Voltage vs. Amplifier Bias Current graph. Larger amplitudes of input signal also improve the S/N ratio. The linearizing diodes help here by allowing larger input signals for the same output distortion as shown by the Distortion vs. Differential Input Voltage graph. S/N may be optimized by adjusting the magnitude of the input signal via R_{IN} (Figure 23) until the output distortion is below some desired level. The output voltage swing can then be set at any level by selecting R_L.

Although the noise contribution of the linearizing diodes is negligible relative to the contribution of the amplifier's internal transistors, I_D should be as large as possible. This minimizes the dynamic junction resistance of the diodes (r_e) and maximizes their linearizing action when balanced against R_{IN}. A value of 1 mA is recommended for I_D unless the specific application demands otherwise.

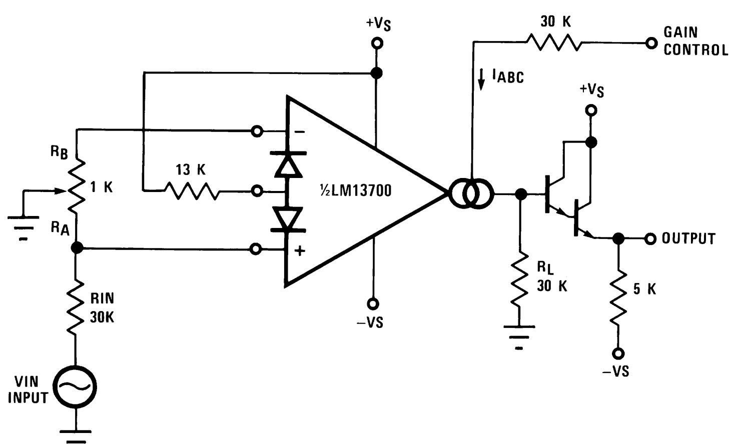


Figure 23. Voltage Controlled Amplifier

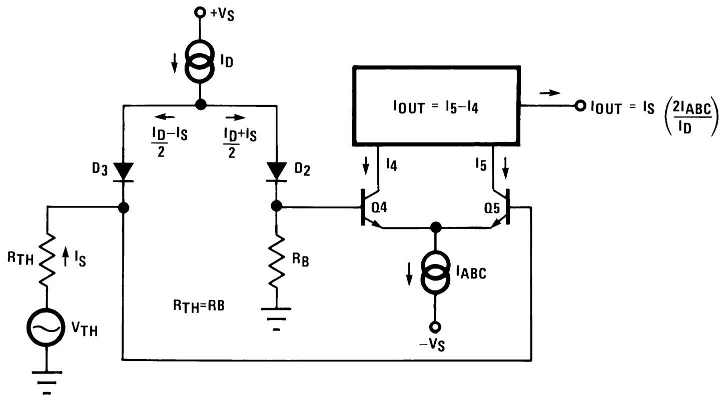


Figure 24. Equivalent VCA Input Circuit

Stereo Volume Control

The circuit of Figure 25 uses the excellent matching of the two LM13700 amplifiers to provide a Stereo Volume Control with a typical channel-to-channel gain tracking of 0.3 dB. R_P is provided to minimize the output offset voltage and may be replaced with two 510Ω resistors in AC-coupled applications. For the component values given, amplifier gain is derived for Figure 23 as being:

$$\frac{V_O}{V_{IN}} = 940 \times I_{ABC} \quad (8)$$

If V_C is derived from a second signal source then the circuit becomes an amplitude modulator or two-quadrant multiplier as shown in Figure 26, where:

$$I_O = \frac{-2I_S}{I_D}(I_{ABC}) = \frac{-2I_S}{I_D}\frac{V_{IN2}}{R_C} - \frac{2I_S}{I_D}\frac{(V^- + 1.4V)}{R_C} \quad (9)$$

The constant term in the above equation may be cancelled by feeding $I_S \times I_D R_C / 2(V^- + 1.4V)$ into I_O. The circuit of Figure 27 adds R_M to provide this current, resulting in a four-quadrant multiplier where R_C is trimmed such that V_O = 0V for V_{IN2} = 0V. R_M also serves as the load resistor for I_O.

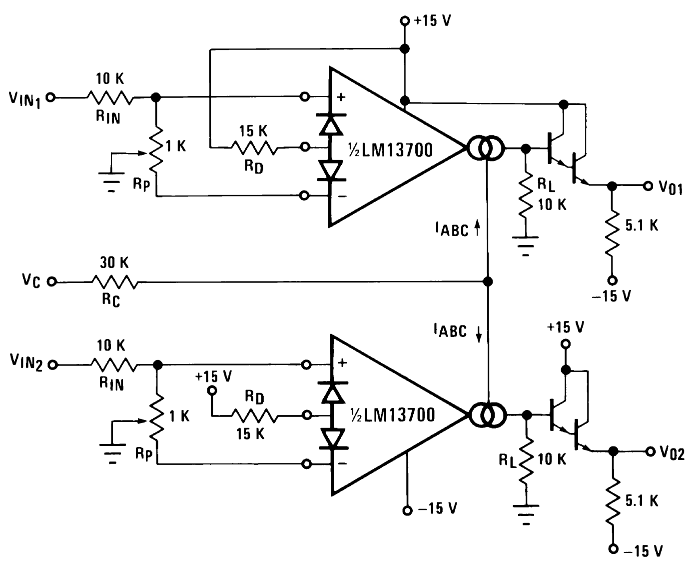


Figure 25. Stereo Volume Control

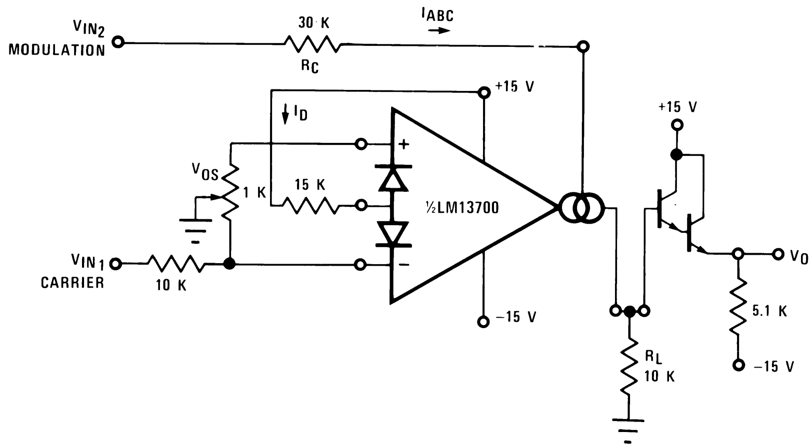


Figure 26. Amplitude Modulator

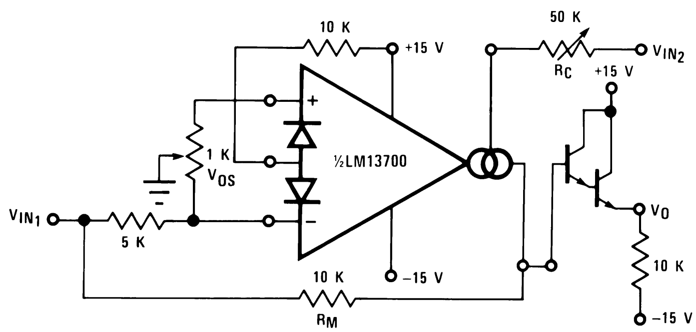


Figure 27. Four-Quadrant Multiplier

Noting that the gain of the LM13700 amplifier of Figure 24 may be controlled by varying the linearizing diode current I_D as well as by varying I_{ABC}, Figure 28 shows an AGC Amplifier using this approach. As V_O reaches a high enough amplitude ($3V_{BE}$) to turn on the Darlington transistors and the linearizing diodes, the increase in I_D reduces the amplifier gain so as to hold V_O at that level.

Voltage Controlled Resistors

An Operational Transconductance Amplifier (OTA) may be used to implement a Voltage Controlled Resistor as shown in Figure 29. A signal voltage applied at R_X generates a V_{IN} to the LM13700 which is then multiplied by the g_m of the amplifier to produce an output current, thus:

$$R_X = \frac{R + R_A}{g_m R_A} \tag{10}$$

where $g_m \approx 19.2 I_{ABC}$ at 25°C. Note that the attenuation of V_O by R and R_A is necessary to maintain V_{IN} within the linear range of the LM13700 input.

Figure 30 shows a similar VCR where the linearizing diodes are added, essentially improving the noise performance of the resistor. A floating VCR is shown in Figure 31, where each “end” of the “resistor” may be at any voltage within the output voltage range of the LM13700.

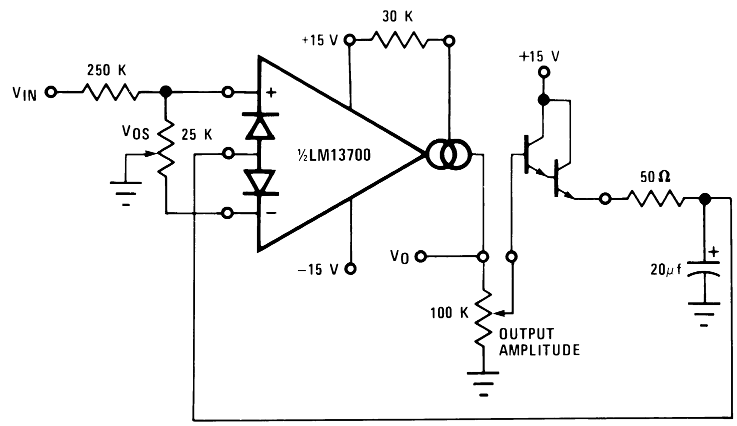


Figure 28. AGC Amplifier

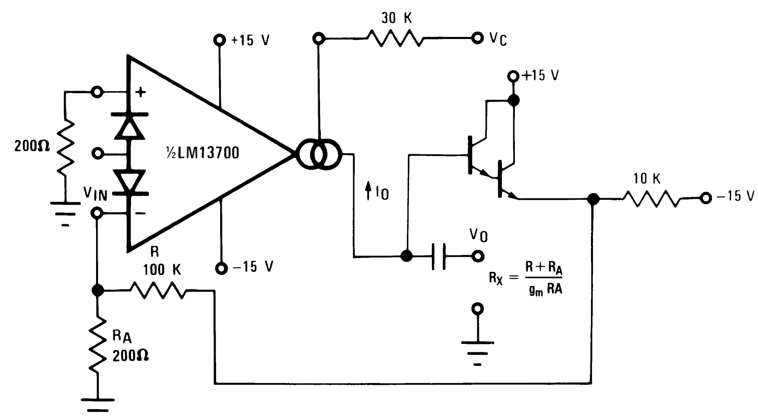


Figure 29. Voltage Controlled Resistor, Single-Ended

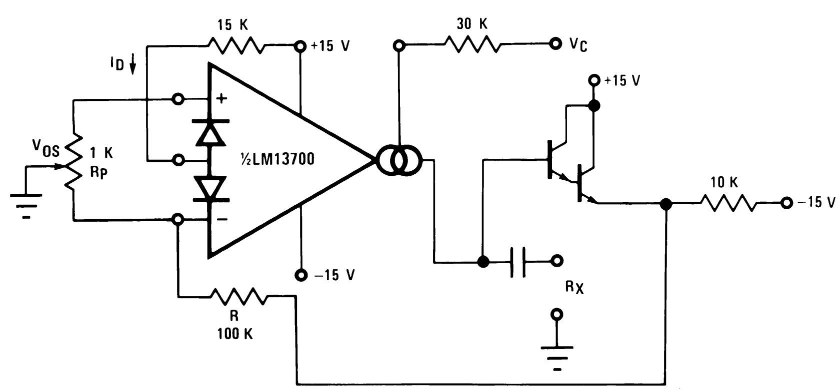


Figure 30. Voltage Controlled Resistor with Linearizing Diodes

Voltage Controlled Filters

OTA's are extremely useful for implementing voltage controlled filters, with the LM13700 having the advantage that the required buffers are included on the I.C. The VC Lo-Pass Filter of Figure 32 performs as a unity-gain buffer amplifier at frequencies below cut-off, with the cut-off frequency being the point at which X_C/g_m equals the closed-loop gain of (R/R_A). At frequencies above cut-off the circuit provides a single RC roll-off (6 dB per octave) of the input signal amplitude with a −3 dB point defined by the given equation, where g_m is again $19.2 \times I_{ABC}$ at room temperature. Figure 33 shows a VC High-Pass Filter which operates in much the same manner, providing a single RC roll-off below the defined cut-off frequency.

Additional amplifiers may be used to implement higher order filters as demonstrated by the two-pole Butterworth Lo-Pass Filter of Figure 34 and the state variable filter of Figure 35. Due to the excellent g_m tracking of the two amplifiers, these filters perform well over several decades of frequency.

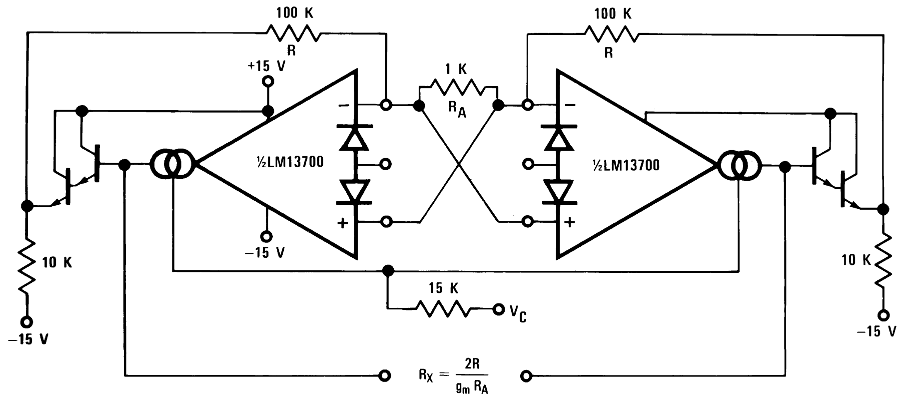


Figure 31. Floating Voltage Controlled Resistor

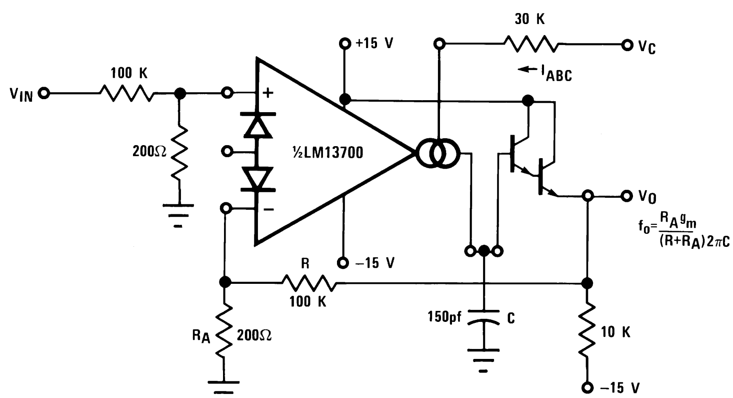
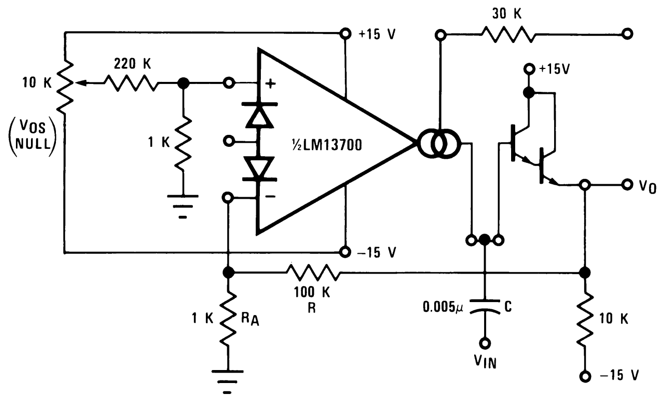
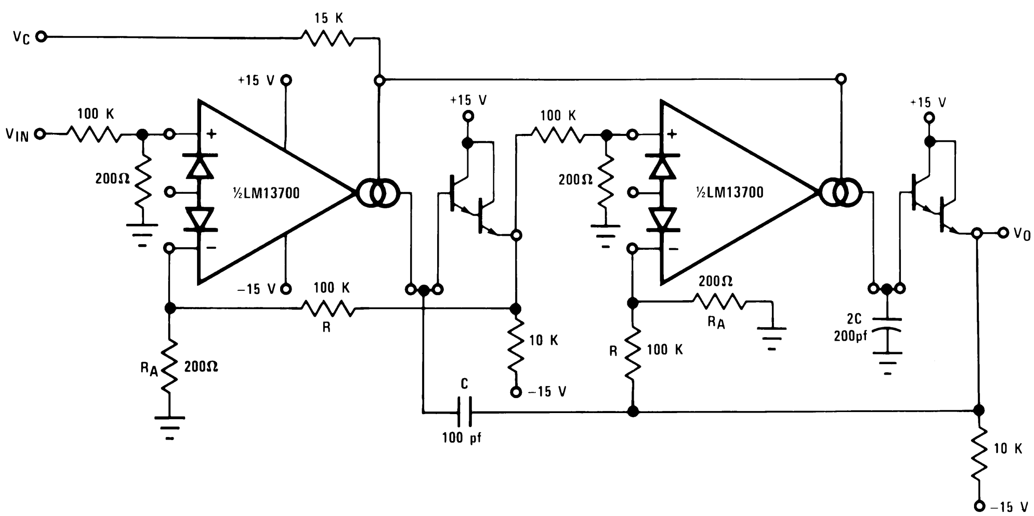


Figure 32. Voltage Controlled Low-Pass Filter



$$f_o = \frac{R_A\, g_m}{(R + R_A)\, 2\pi C}$$

Figure 33. Voltage Controlled Hi-Pass Filter



$$f_o = \frac{R_A\, g_m}{(R + R_A)\, 2\pi C}$$

Figure 34. Voltage Controlled 2-Pole Butterworth Lo-Pass Filter

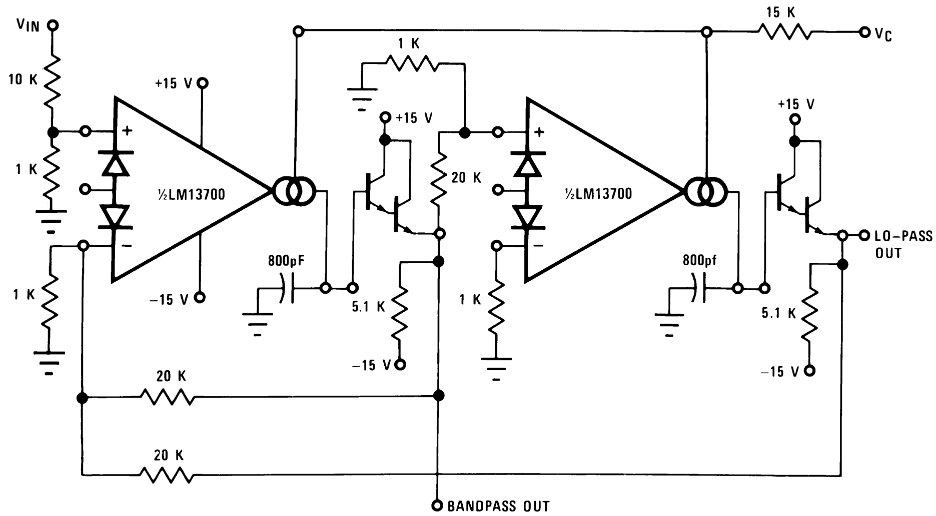


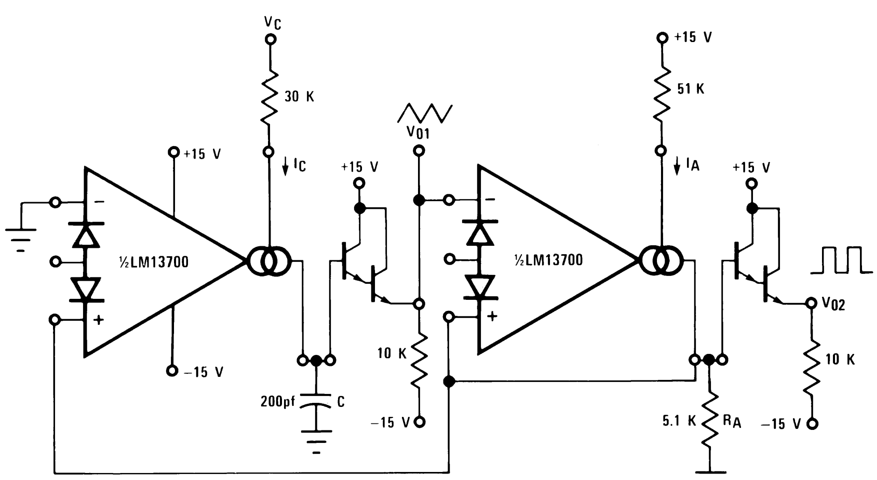
Figure 35. Voltage Controlled State Variable Filter

Voltage Controlled Oscillators

The classic Triangular/Square Wave VCO of Figure 36 is one of a variety of Voltage Controlled Oscillators which may be built utilizing the LM13700. With the component values shown, this oscillator provides signals from 200 kHz to below 2 Hz as I_C is varied from 1 mA to 10 nA. The output amplitudes are set by $I_A \times R_A$. Note that the peak differential input voltage must be less than 5V to prevent zenering the inputs.

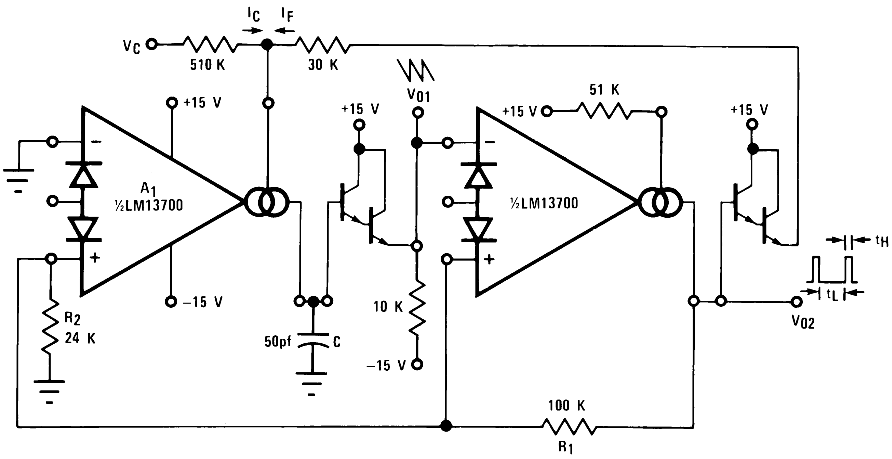
A few modifications to this circuit produce the ramp/pulse VCO of Figure 37. When V_{O2} is high, I_F is added to I_C to increase amplifier A1's bias current and thus to increase the charging rate of capacitor C. When V_{O2} is low, I_F goes to zero and the capacitor discharge current is set by I_C.

The VC Lo-Pass Filter of Figure 32 may be used to produce a high-quality sinusoidal VCO. The circuit of Figure 37 employs two LM13700 packages, with three of the amplifiers configured as lo-pass filters and the fourth as a limiter/inverter. The circuit oscillates at the frequency at which the loop phase-shift is 360° or 180° for the inverter and 60° per filter stage. This VCO operates from 5 Hz to 50 kHz with less than 1% THD.



$$f_{OSC} = \frac{I_C}{4CI_AR_A}$$

Figure 36. Triangular/Square-Wave VCO



$$V_{PK} = \frac{(V^+ \pm 0.8V)\, R_2}{R_1 + R_2}$$

$$t_H \approx \frac{2V_{PK}C}{I_F}$$

$$t_L = \frac{2V_{PK}C}{I_C}$$

$$f_0 \approx \frac{I_C}{2V_{PK}C} \text{ for } I_C << I_F$$

Figure 37. Ramp/Pulse VCO

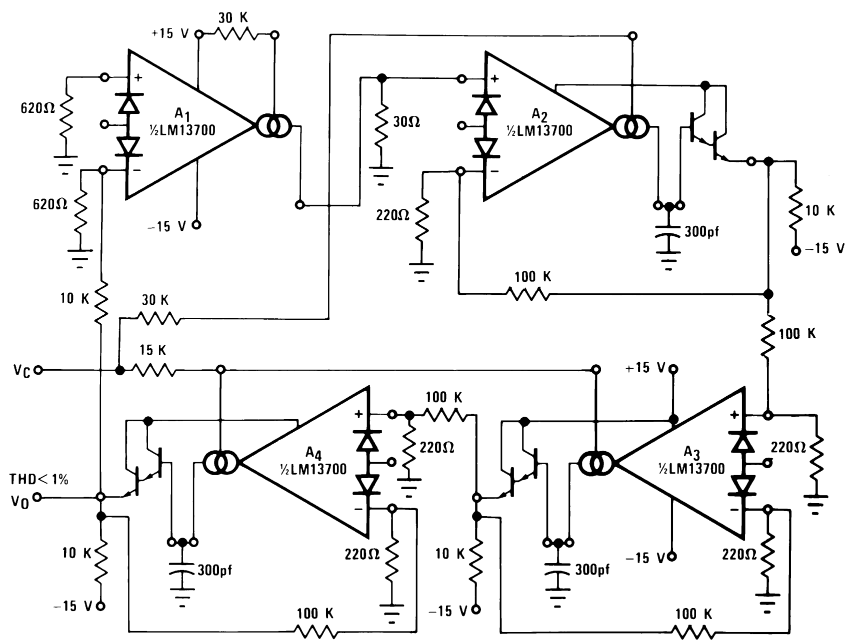


Figure 38. Sinusoidal VCO

Figure 39 shows how to build a VCO using one amplifier when the other amplifier is needed for another function.

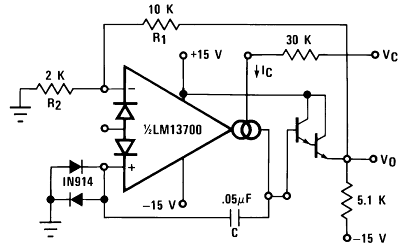


Figure 39. Single Amplifier VCO

Additional Applications

Figure 40 presents an interesting one-shot which draws no power supply current until it is triggered. A positive-going trigger pulse of at least 2V amplitude turns on the amplifier through R_B and pulls the non-inverting input high. The amplifier regenerates and latches its output high until capacitor C charges to the voltage level on the non-inverting input. The output then switches low, turning off the amplifier and discharging the capacitor. The capacitor discharge rate is speeded up by shorting the diode bias pin to the inverting input so that an additional discharge current flows through D_I when the amplifier output switches low. A special feature of this timer is that the other amplifier, when biased from V_O, can perform another function and draw zero stand-by power as well.

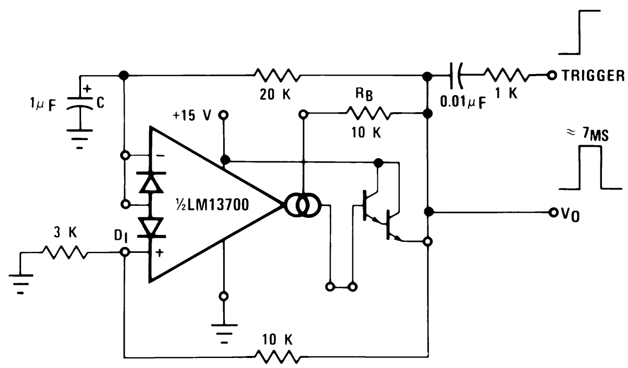


Figure 40. Zero Stand-By Power Timer

The operation of the multiplexer of Figure 41 is very straightforward. When A1 is turned on it holds V_O equal to V_{IN1} and when A2 is supplied with bias current then it controls V_O. C_C and R_C serve to stabilize the unity-gain configuration of amplifiers A1 and A2. The maximum clock rate is limited to about 200 kHz by the LM13700 slew rate into 150 pF when the (V_{IN1}–V_{IN2}) differential is at its maximum allowable value of 5V.

The Phase-Locked Loop of Figure 42 uses the four-quadrant multiplier of Figure 27 and the VCO of Figure 39 to produce a PLL with a ±5% hold-in range and an input sensitivity of about 300 mV.

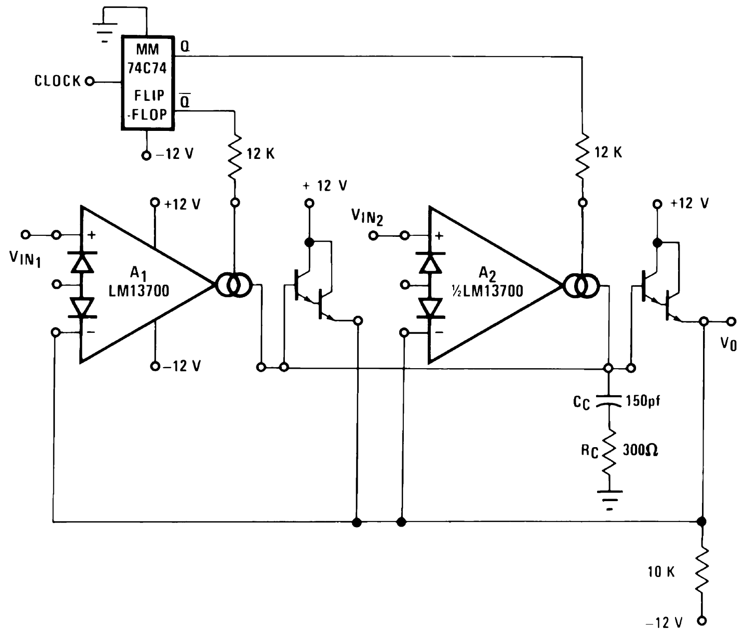


Figure 41. Multiplexer

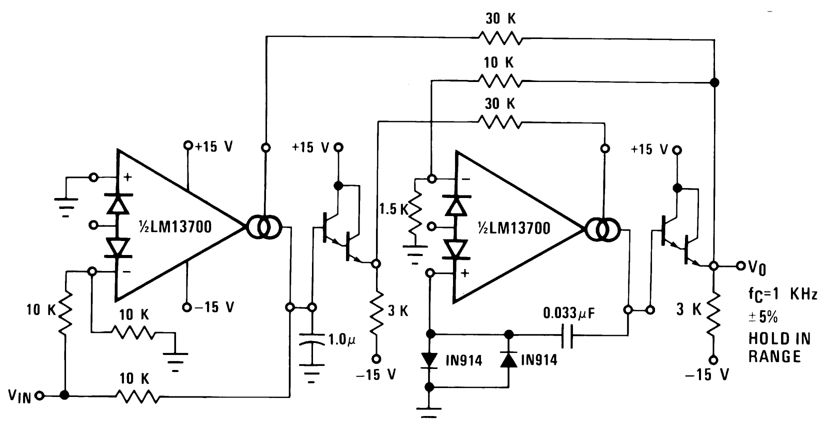


Figure 42. Phase Lock Loop

The Schmitt Trigger of Figure 43 uses the amplifier output current into R to set the hysteresis of the comparator; thus $V_H = 2 \times R \times I_B$. Varying I_B will produce a Schmitt Trigger with variable hysteresis.

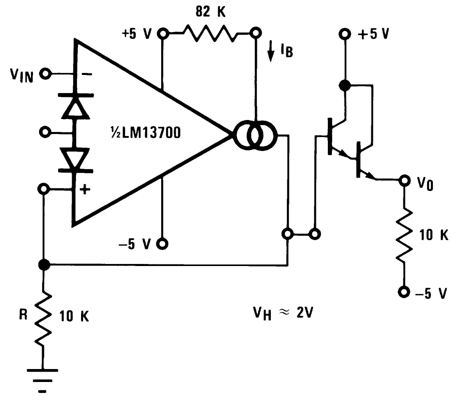


Figure 43. Schmitt Trigger

Figure 44 shows a Tachometer or Frequency-to-Voltage converter. Whenever A1 is toggled by a positive-going input, an amount of charge equal to $(V_H – V_L)\ C_t$ is sourced into C_f and R_t. This once per cycle charge is then balanced by the current of V_O/R_t. The maximum F_{IN} is limited by the amount of time required to charge C_t from V_L to V_H with a current of I_B, where V_L and V_H represent the maximum low and maximum high output voltage swing of the LM13700. D1 is added to provide a discharge path for C_t when A1 switches low.

The Peak Detector of Figure 45 uses A2 to turn on A1 whenever V_{IN} becomes more positive than V_O. A1 then charges storage capacitor C to hold V_O equal to V_{IN} PK. Pulling the output of A2 low through D1 serves to turn off A1 so that V_O remains constant.

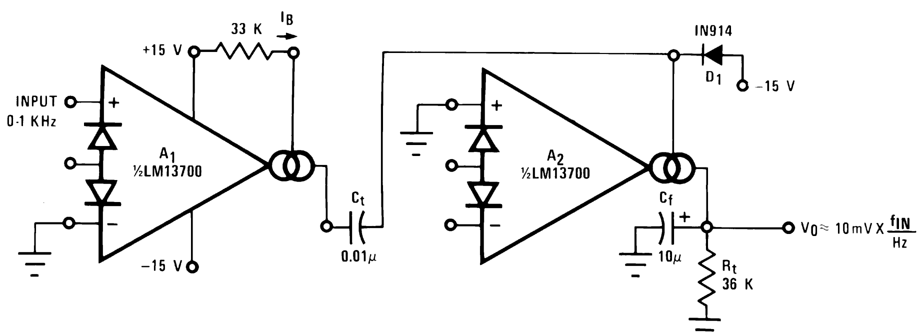


Figure 44. Tachometer

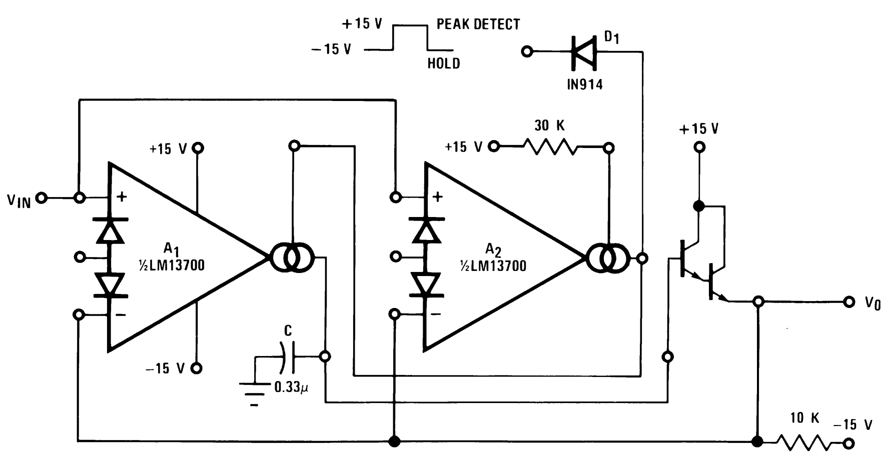


Figure 45. Peak Detector and Hold Circuit

The Ramp-and-Hold of Figure 47 sources I_B into capacitor C whenever the input to A1 is brought high, giving a ramp-rate of about 1V/ms for the component values shown.

The true-RMS converter of Figure 48 is essentially an automatic gain control amplifier which adjusts its gain such that the AC power at the output of amplifier A1 is constant. The output power of amplifier A1 is monitored by squaring amplifier A2 and the average compared to a reference voltage with amplifier A3. The output of A3 provides bias current to the diodes of A1 to attenuate the input signal. Because the output power of A1 is held constant, the RMS value is constant and the attenuation is directly proportional to the RMS value of the input voltage. The attenuation is also proportional to the diode bias current. Amplifier A4 adjusts the ratio of currents through the diodes to be equal and therefore the voltage at the output of A4 is proportional to the RMS value of the input voltage. The calibration potentiometer is set such that V_O reads directly in RMS volts.

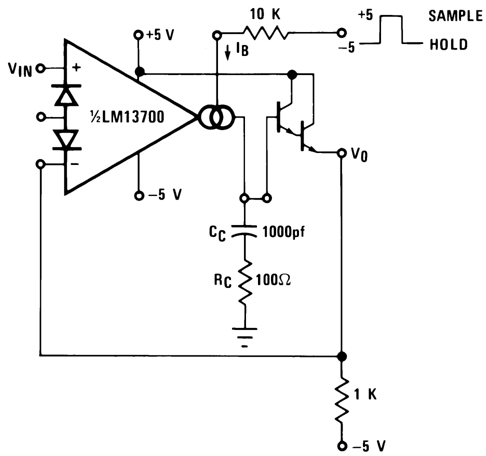


Figure 46. Sample-Hold Circuit

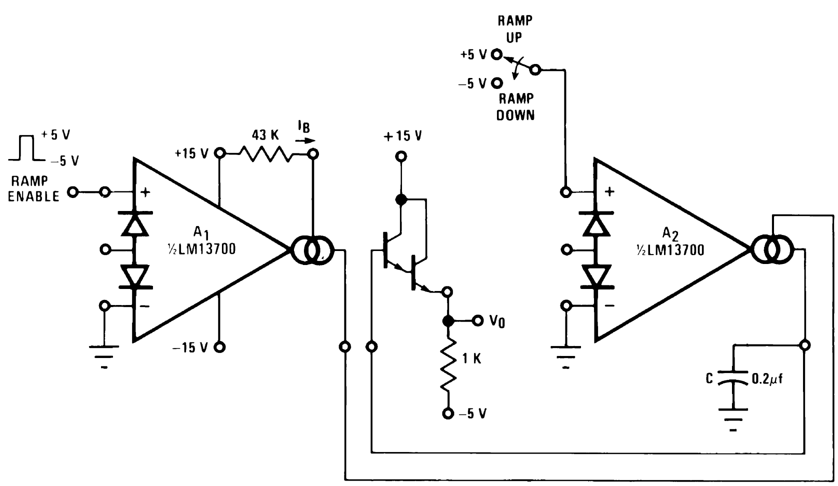


Figure 47. Ramp and Hold

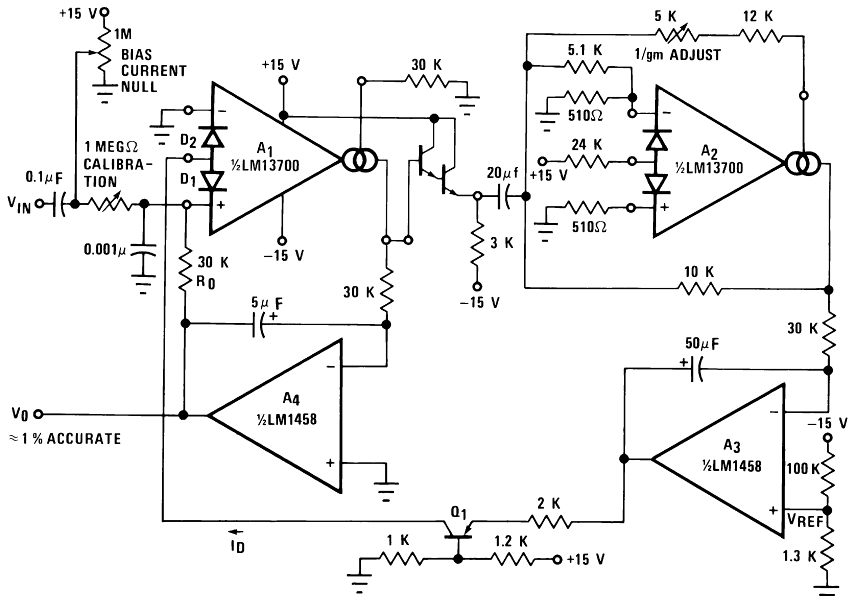


Figure 48. True RMS Converter

The circuit of Figure 49 is a voltage reference of variable Temperature Coefficient. The 100 kΩ potentiometer adjusts the output voltage which has a positive TC above 1.2V, zero TC at about 1.2V, and negative TC below 1.2V. This is accomplished by balancing the TC of the A2 transfer function against the complementary TC of D1.

The wide dynamic range of the LM13700 allows easy control of the output pulse width in the Pulse Width Modulator of Figure 50.

For generating I_{ABC} over a range of 4 to 6 decades of current, the system of Figure 51 provides a logarithmic current out for a linear voltage in.

Since the closed-loop configuration ensures that the input to A2 is held equal to 0V, the output current of A1 is equal to $I_3 = -V_C/R_C$.

The differential voltage between Q1 and Q2 is attenuated by the R1,R2 network so that A1 may be assumed to be operating within its linear range. From Equation 5, the input voltage to A1 is:

$$V_{IN}1 = \frac{-2kTI_3}{qI_2} = \frac{-2kTV_C}{qI_2R_C} \tag{11}$$

The voltage on the base of Q1 is then

$$V_B1 = \frac{(R_1 + R_2)\,V_{IN}1}{R_1} \tag{12}$$

The ratio of the Q1 and Q2 collector currents is defined by:

$$V_B1 = \frac{kT}{q} \ln \frac{I_{C2}}{I_{C1}} \approx \frac{kT}{q} \ln \frac{I_{ABC}}{I_1} \tag{13}$$

Combining and solving for I_{ABC} yields:

$$I_{ABC} = I_1 \exp \frac{2(R_1 + R_2)\,V_C}{R_1\,I_2\,R_C} \tag{14}$$

This logarithmic current can be used to bias the circuit of Figure 25 to provide temperature independent stereo attenuation characteristic.

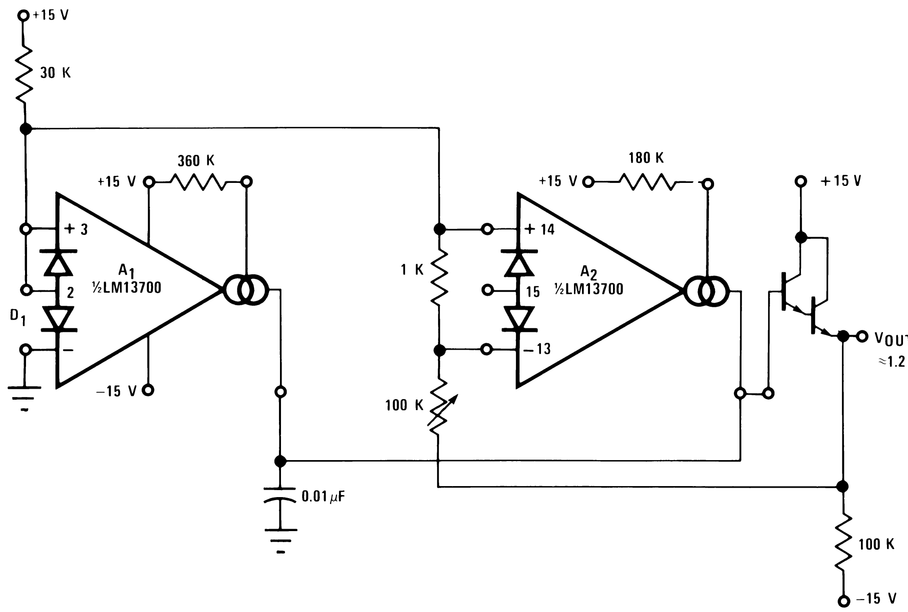


Figure 49. Delta VBE Reference

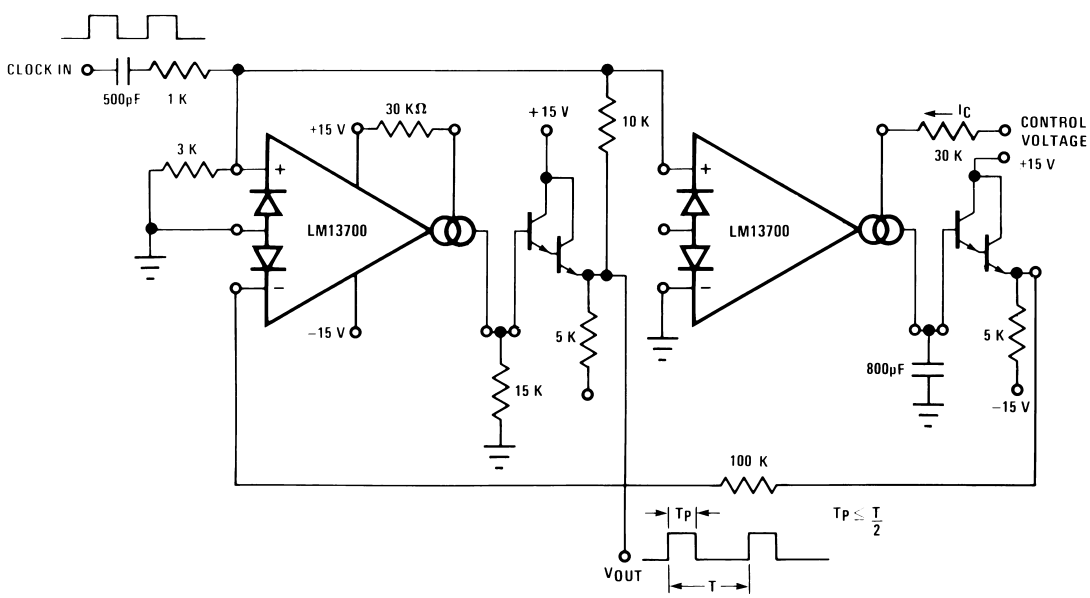
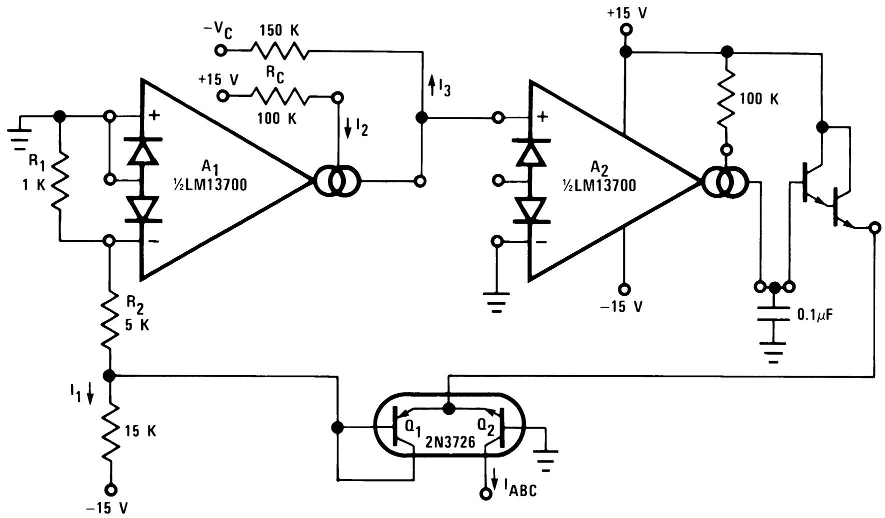


Figure 50. Pulse Width Modulator



$I_{ABC} = I_1 \exp \frac{-CI_3}{I_2}$

Figure 51. Logarithmic Current Source

REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	24

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM13700M	NRND	SOIC	D	16	48	TBD	Call TI	Call TI	0 to 70	LM13700M	
LM13700M/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM13700M	Samples
LM13700MX	NRND	SOIC	D	16	2500	TBD	Call TI	Call TI	0 to 70	LM13700M	
LM13700MX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM13700M	Samples
LM13700N	NRND	PDIP	NFG	16	25	TBD	Call TI	Call TI	0 to 70	LM13700N	
LM13700N/NOPB	ACTIVE	PDIP	NFG	16	25	Pb-Free (RoHS)	CU SN	Level-1-NA-UNLIM	0 to 70	LM13700N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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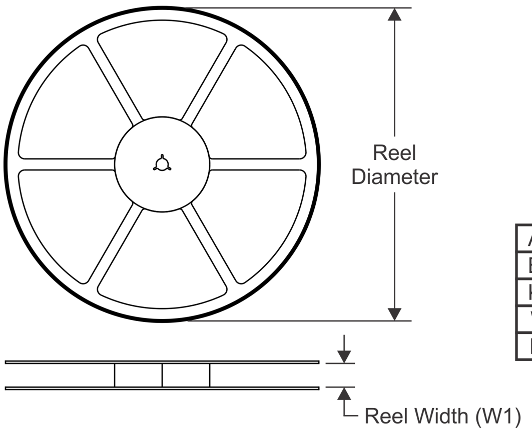
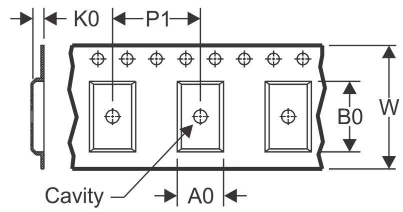
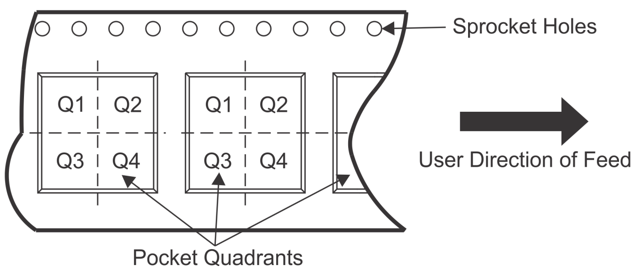




A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

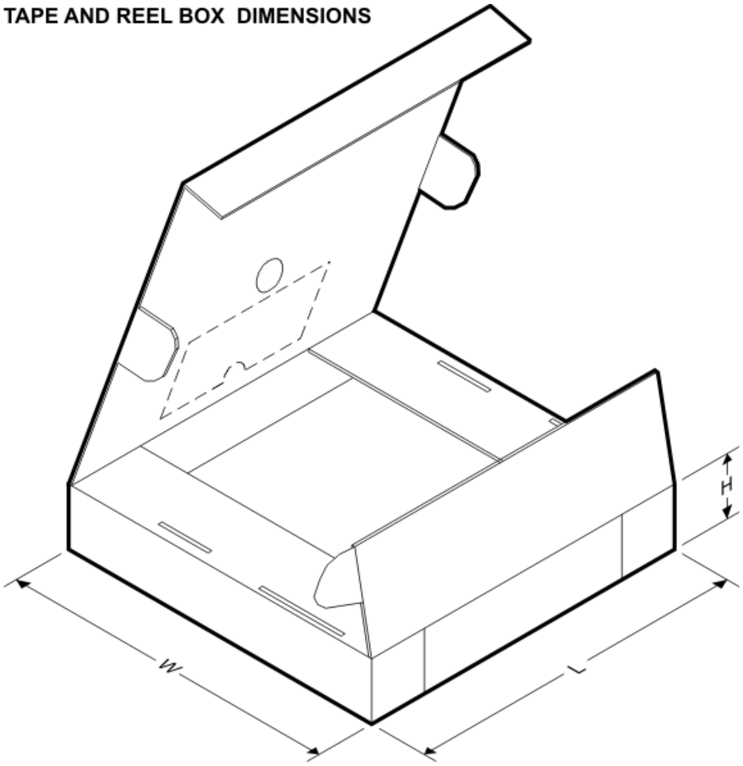
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM13700MX	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
LM13700MX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

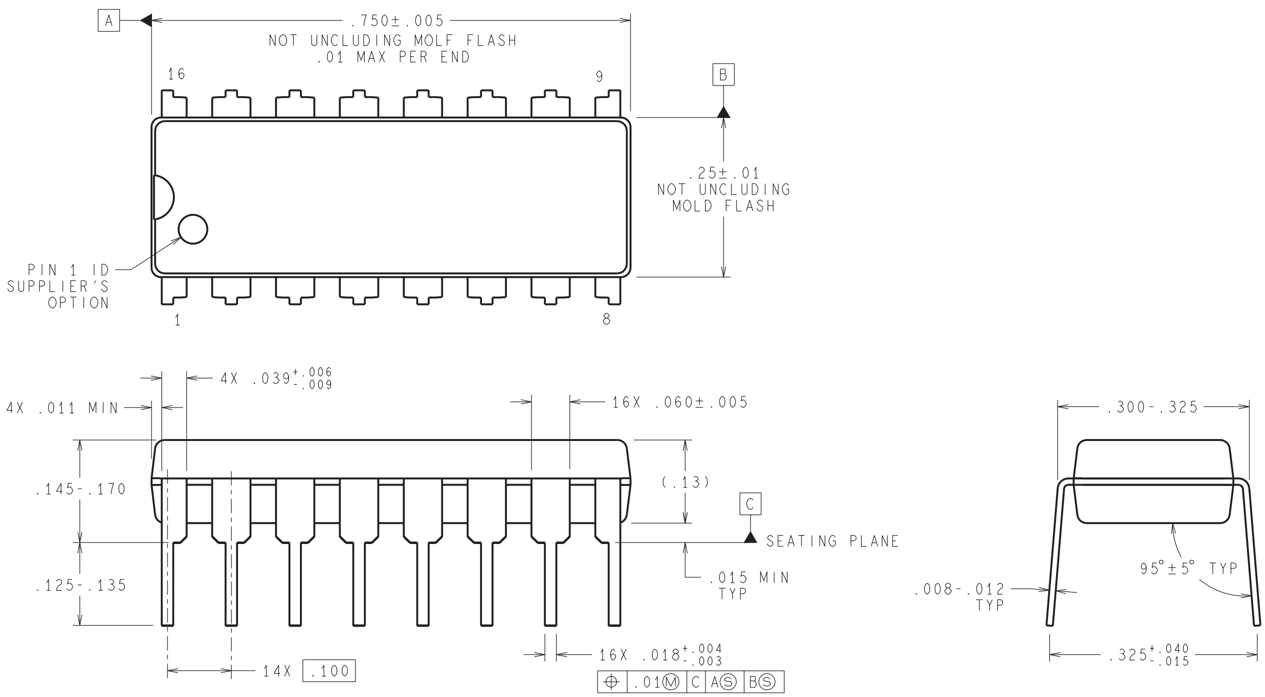
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM13700MX	SOIC	D	16	2500	367.0	367.0	35.0
LM13700MX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

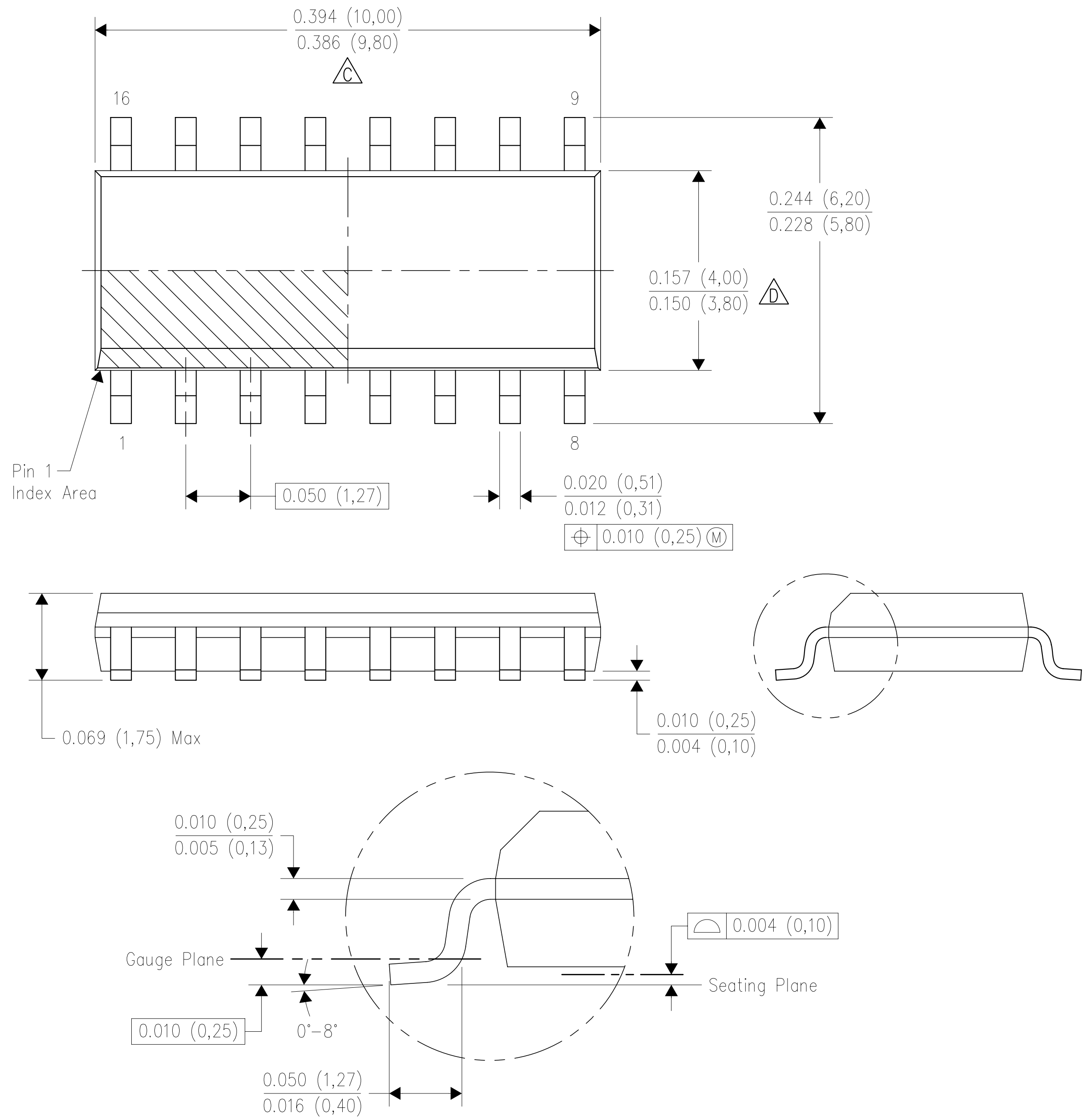
NFG0016E



DIMENSIONS ARE IN INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

N16E (Rev G)

D (R-PDSO-G16) PLASTIC SMALL OUTLINE



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NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

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